AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) An electrostatic discharge (ESD) NMOSFET with a lower trigger voltage comprising:

a substrate having first, second and third wells formed in said substrate, and separated by shallow trench isolation structures, and generally separating the bottom of said second well from said substrate with a segmented conductive band;

a source and drain region in said first well forming an FET, said drain being connected to an I/O pad for protecting said pad against an ESD event; and

a path of substrate material extending through a single opening in said segmented conductive band configured to increase substrate resistance by creating a single extended ~~in the~~ path for current which flows through said I/O pad to substrate contacts and drain during an ESD event and electrically connecting the first well to the substrate,

wherein the second and third wells are completely isolated from the drain, source and substrate contacts by shallow trench isolation structures, and

wherein the substrate contacts are located outside the first, second and third wells and directly connected to the substrate.

2. (Canceled).

3. (Original) An ESD NMOSFET according to claim 1 wherein said first and third wells are N-wells and said conductive band region comprises a semiconductor region which is N doped.

4. (Original) An ESD NMOSFET according to claim 3 wherein said conductive band region is segmented forming said resistive path to said substrate.

5. (Original) The ESD NMOSFET according to claim 1 wherein said FET has a gate connection and source connected to said substrate contact.

6. (Original) The ESD NMOSFET according to claim 1 wherein said drain is connected through a matching impedance to said I/O pad to provide a signal from a circuit on said substrate to said I/O pad.

7. (Currently amended) A method for decreasing the trigger voltage of an ESD NMOSFET comprising:

locating said ESD NMOSFET in a well of a triple well CMOS structure;

connecting said ESD NMOSFET to an I/O pad; and

providing a resistive path extending through a single opening in a segmented conductive band from said well to substrate contacts located outside of said wells, whereby the trigger voltage of the said ESD NMOSFET is ~~reduced~~ minimized due to the length of said resistive path between said substrate contacts and said I/O pad and

wherein a first, second and third wells are formed in a substrate of the triple well CMOS structure,

wherein a second well and third well of the triple well CMOS structure are completely isolated from a drain and source of the ESD NMOSFET by shallow trench isolation structures, and

wherein the substrate contacts are located outside the first, second and third wells, completely isolated from the drain and source of the ESD NMOSFET and directly connected to the substrate.

8. (Original) The method according to claim 7 wherein said resistive path is an opening in said well to form a connection between said NMOSFET and said substrate contact.

9. (Previously presented) The method according to claim 7 wherein said well is a P-well with an N-band of N doped semiconductor material which separates said P-well from said substrate, and which includes an opening forming said resistive path.

10. (Original) The method according to claim 7 wherein said ESD NMOSFET further comprising connecting a gate connection and a source of said NMOSFET to said substrate contact.

11. (Previously presented) The method according to claim 7 wherein a second and third well of said triple well structure are N-Wells, and one of said N-wells is connected to a voltage.

12. (Previously presented) The method according to claim 7 further comprising connecting a gate of said NMOSFET to said substrate contact.

13. (Currently amended) An ESD NMOSFET with a lower trigger voltage comprising:

substrate having first, second and third wells formed in said substrate, said first well comprising a P-well, said first well separated from said substrate along a bottom thereof with a segmented conductive band region;

substrate contacts located outside of said first, second and third wells and the substrate contacts are directly connected to the substrate;

a source and drain region in said first well and forming an FET, said drain being connected to an I/O pad for protecting said I/O pad against an ESD event and said drain and source are isolated from second and third N-Wells by shallow trench isolation structures; and

a resistive path extending through a single opening in said segmented conductive band region to said substrate contacts, said resistive path ~~decreasing~~ minimizing the trigger voltage for said FET.

14. (Previously presented) The ESD NMOSFET according to claim 13 wherein said FET source and gate are connected to said substrate contacts.

15. (Previously presented) The ESD NMOSFET according to claim 13 wherein said source is connected to said substrate contacts.

16. (Previously presented) The ESD NMOSFET according to claim 1 further comprising silicide blocked regions formed over the source and drain.

17. (Previously presented) The method for decreasing the trigger voltage of an ESD NMOSFET according to claim 7 comprising silicide blocked regions formed over the source and drain.

18. (Previously presented) The ESD NMOSFET according to claim 13 further comprising silicide blocked regions formed over the source and drain.